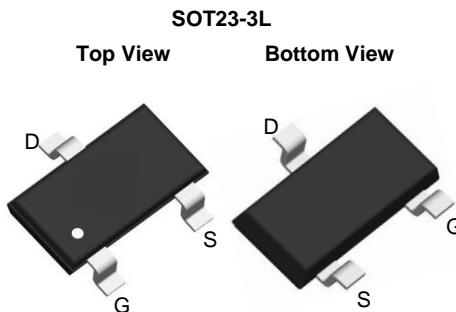


N-Channel Enhancement Mode MOSFET
Features

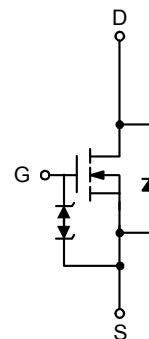
- 30V/5.7A
- $R_{DS(ON)}=19\text{m}\Omega$ (typ) @ $VGS=10\text{V}$
 $R_{DS(ON)}=25\text{m}\Omega$ (typ) @ $VGS=4.5\text{V}$
- 100% UIS & RG Tested
- Reliable and Rugged
- Lead Free and Green Devices Available
(RoHS Compliant)


Applications

- Power Management for Industrial DC/DC Converters

Marking

Marking	X4****
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N-Channel MOSFET
Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Rating	Unit
Common Ratings			
V_{DSS}	Drain-Source Voltage	30	V
V_{GSS}	Gate-Source Voltage	± 20	
I_D	Continuous Drain Current	5.7	A
I_{DM}	Pulsed Drain Current	64	
I_S	Diode Continuous Forward Current	1.7	A
T_{STG}, T_j	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
PD	Power Dissipation	$T_A=25^\circ\text{C}$	W
		$T_A=70^\circ\text{C}$	
$R_{\theta JA}$	Thermal Resistance-Junction to Ambient	90	$^\circ\text{C}/\text{W}$

Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Static Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{\text{GS}}=0\text{V}, I_{\text{DS}}=250\mu\text{A}$	30	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{\text{DS}}=24\text{V}, V_{\text{GS}}=0\text{V}$	-	-	1	μA
		$T_J=55^\circ\text{C}$			30	
$V_{\text{GS}(\text{th})}$	Gate Threshold Voltage	$V_{\text{DS}}=V_{\text{GS}}, I_{\text{DS}}=250\mu\text{A}$	0.5	-	1	V
I_{GSS}	Gate Leakage Current	$V_{\text{GS}}=\pm 20\text{V}, V_{\text{DS}}=0\text{V}$	-	-	± 100	nA
$R_{\text{DS}(\text{ON})}$	Drain-Source On-state Resistance	$V_{\text{GS}}=10\text{V}, I_{\text{DS}}=5.7\text{A}$	-	19	25	$\text{m}\Omega$
		$V_{\text{GS}}=4.5\text{V}, I_{\text{DS}}=5\text{A}$	-	25	35	
Body Diode Characteristics						
V_{SD}	Diode Forward Voltage	$I_{\text{SD}}=1\text{A}, V_{\text{GS}}=0\text{V}$	-	0.7	1.0	V
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{\text{GS}}=0\text{V}, V_{\text{DS}}=15\text{V},$ $\text{Frequency}=1.0\text{MHz}$	-	416	-	pF
C_{oss}	Output Capacitance		-	62	-	
C_{rss}	Reverse transfer capacitance		-	40	-	
$t_{\text{d}(\text{ON})}$	Turn-on delay Time	$V_{\text{GS}}=10\text{V}, V_{\text{DS}}=15\text{V}$ $R_G=6\Omega, I_D=1\text{A}, R_L=10\Omega,$	-	7	15	nS
t_r	Turn-on rise Time		-	10	20	
$t_{\text{d}(\text{OFF})}$	Turn-off delay Time		-	20	40	
t_f	Turn-off rise Time		-	11	20	
Gate Charge Characteristics						
Q_g	Total Gate Charge	$V_{\text{DS}}=15\text{V}, V_{\text{GS}}=10\text{V},$ $I_{\text{DS}}=5.7\text{A}$	-	10	-	nC
Q_{gs}	Gate-Source Charge		-	1.7	-	
Q_{gd}	Gate-Drain Charge		-	3.2	-	

TYPICAL CHARACTERISTICS (25 °C Unless Note)

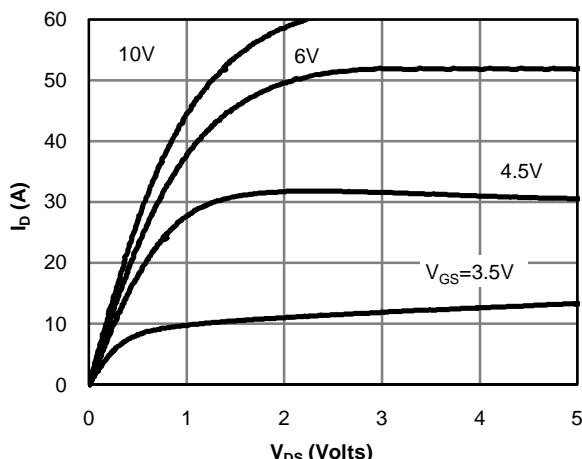


Fig 1: On-Region Characteristics

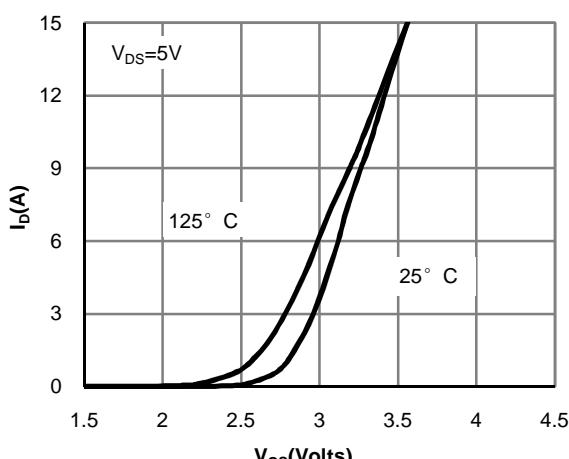


Figure 2: Transfer Characteristics

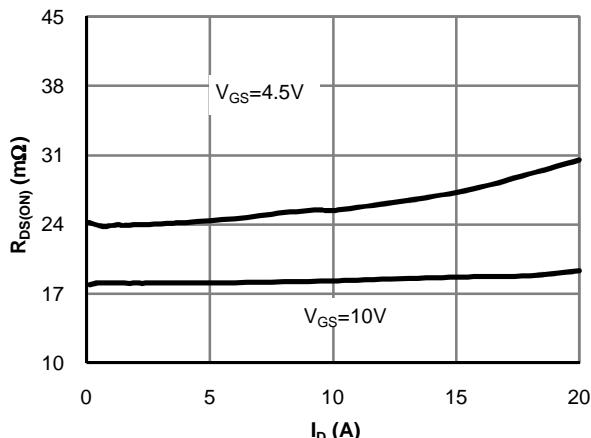


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

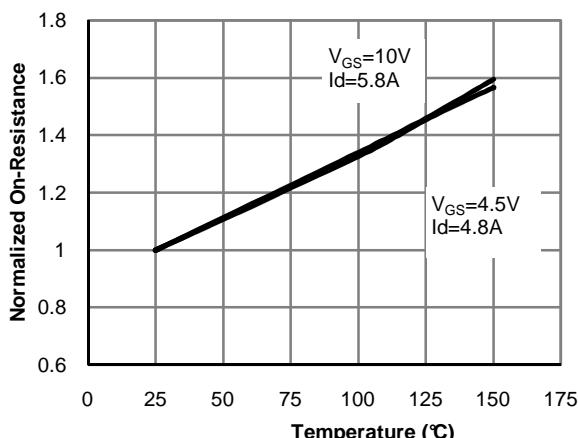


Figure 4: On-Resistance vs. Junction Temperature

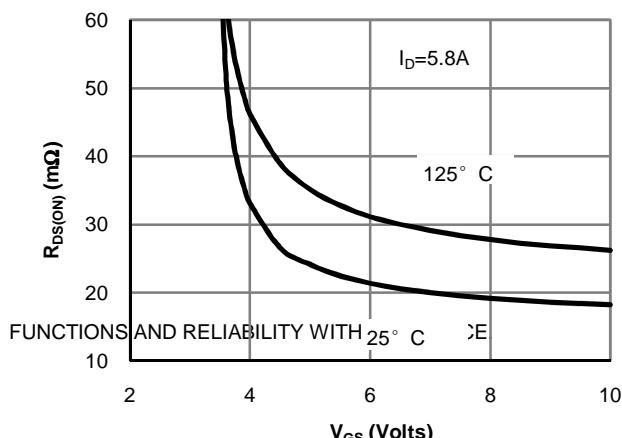


Figure 5: On-Resistance vs. Gate-Source Voltage

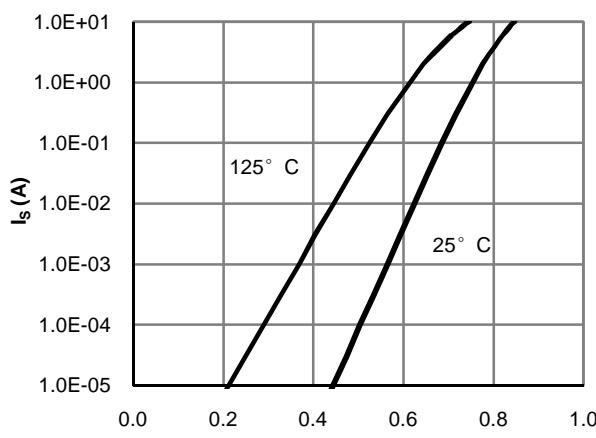


Figure 6: Body-Diode Characteristics

TYPICAL CHARACTERISTICS (continuous)

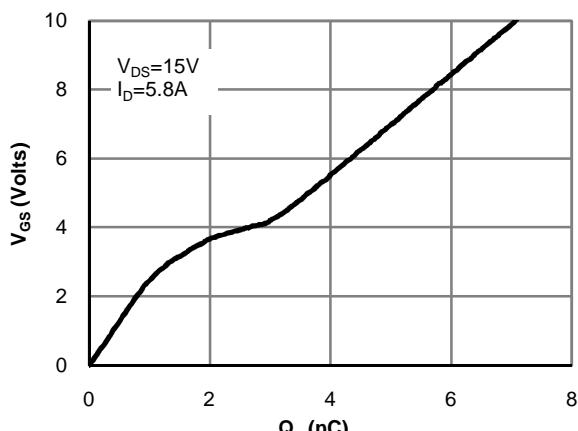


Figure 7: Gate-Charge Characteristics

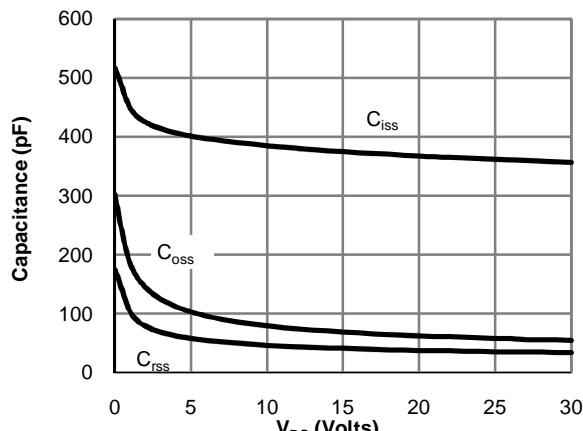


Figure 8: Capacitance Characteristics

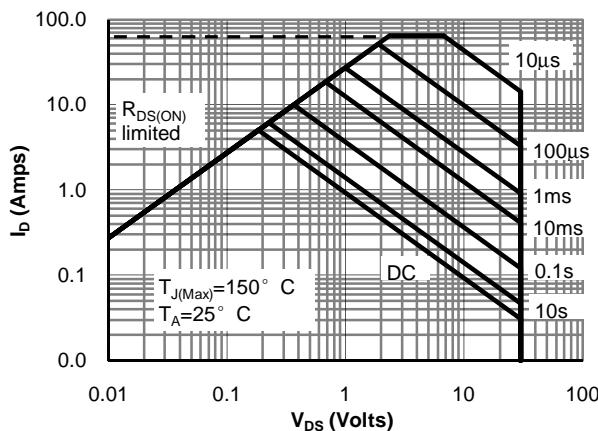


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

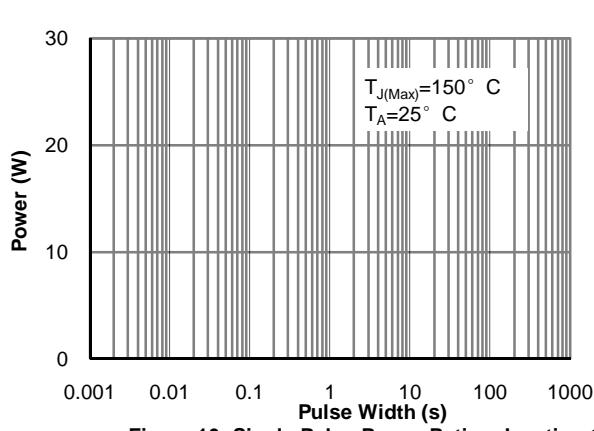


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

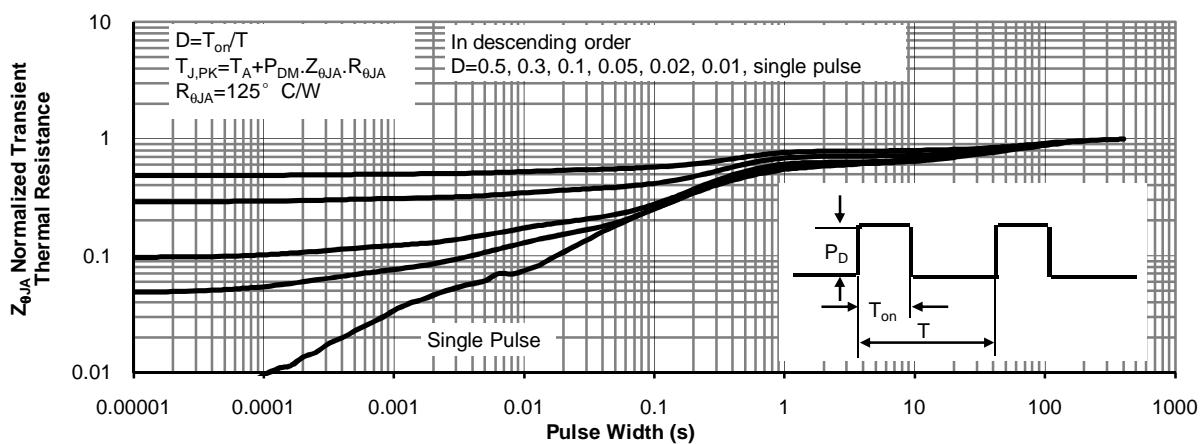
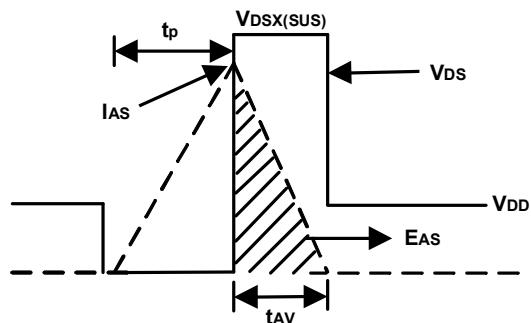
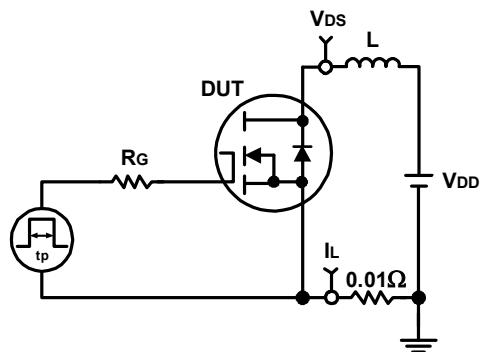
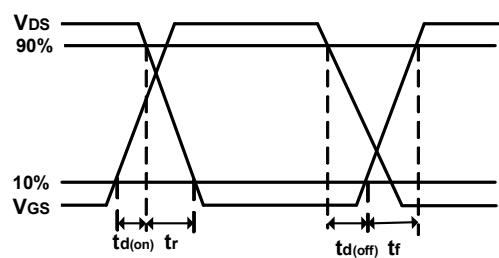
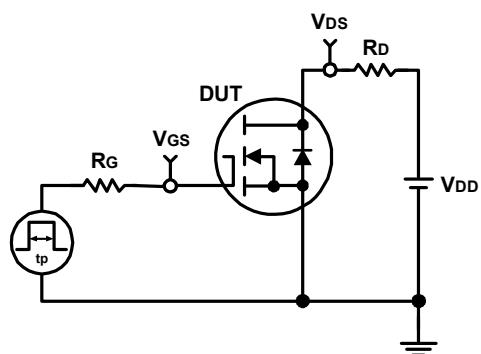


Figure 11: Normalized Maximum Transient Thermal Impedance

Avalanche Test Circuit and Waveforms

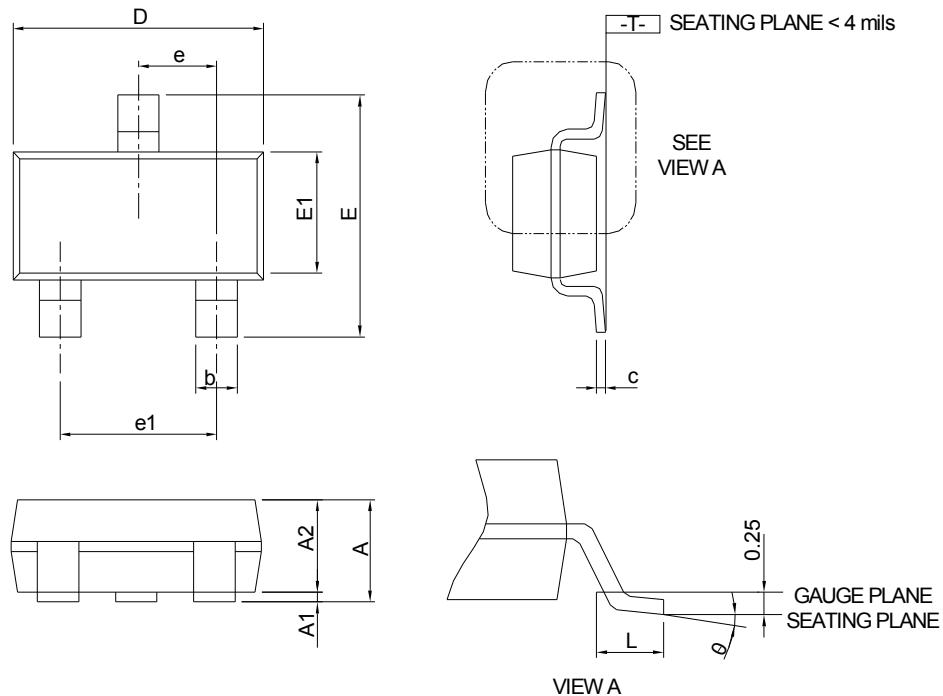


Switching Time Test Circuit and Waveforms



Package Information

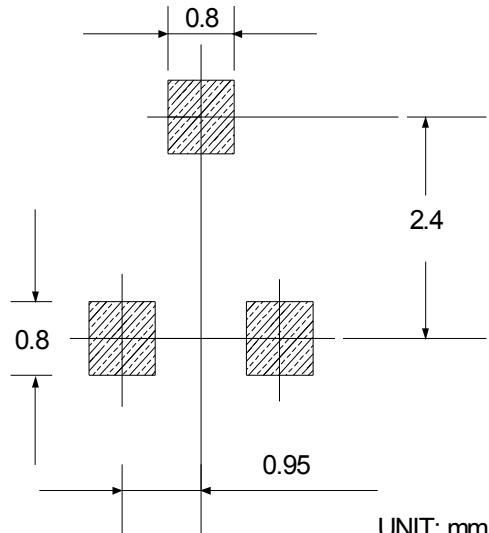
SOT23-3L



SYMBOL	SOT23-3L			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.20		0.047
A1	0.00	0.08	0.000	0.003
A2	0.90	1.12	0.035	0.044
b	0.30	0.50	0.012	0.020
c	0.08	0.22	0.003	0.009
D	2.70	3.10	0.106	0.122
E	2.60	3.00	0.102	0.118
E1	1.40	1.80	0.055	0.071
e	0.95 BSC		0.037 BSC	
e1	1.90 BSC		0.075 BSC	
L	0.30	0.60	0.012	0.024
θ	0°	8°	0°	8°

Note : Dimension D and E1 do not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 10 mil per side.

RECOMMENDED LAND PATTERN



Attention

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