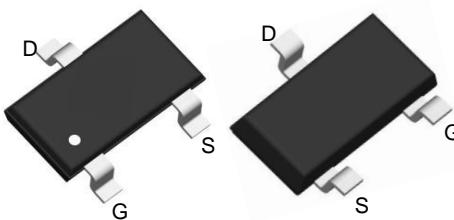


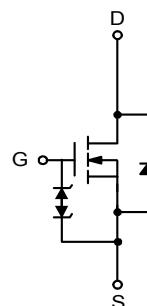
**N-Channel Enhancement Mode MOSFET**
**Features**

- 55V/2.1A
- $R_{DS(ON)}=90\text{m}\Omega$  (typ) @ $V_{GS}=4.5\text{V}$
- $R_{DS(ON)}=154\text{m}\Omega$  (typ) @ $V_{GS}=2.5\text{V}$
- 100% UIS & RG Tested
- Reliable and Rugged
- Lead Free and Green Devices Available (RoHS Compliant)

SOT23-3L  
Top View      Bottom View


**Applications**

- Power Management for Industrial DC/DC Converters



N-Channel MOSFET

**Marking**

Marking	AR****
---------	--------

**Absolute Maximum Ratings** ( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Symbol	Parameter		Rating	Unit
<b>Common Ratings</b>				
$V_{DSS}$	Drain-Source Voltage	$V_{GS}=4.5\text{V}$	55	V
$V_{GSS}$	Gate-Source Voltage		$\pm 12$	
$I_D$	Continuous Drain Current( $T_J=150^\circ\text{C}$ )	$V_{GS}=4.5\text{V}$	2.1	A
$I_{DM}$	Pulsed Drain Current		10	
$I_S$	Diode Continuous Forward Current		1	A
$T_{STG}, T_j$	Storage Temperature Range		-55 to 150	
PD	Power Dissipation	$T_A=25^\circ\text{C}$	1.25	W
		$T_A=70^\circ\text{C}$	0.8	
$R_{\theta JA}$	Thermal Resistance-Junction to Ambient	62.5		°C/W

**Electrical Characteristics** ( $T_A = 25^\circ\text{C}$  Unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static Characteristics</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0\text{V}, I_{DS}=250\mu\text{A}$	55	-	-	V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS}=44\text{V}, V_{GS}=0\text{V}$	-	-	1	$\mu\text{A}$
		$T_j=55^\circ\text{C}$			5	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_{DS}=250\mu\text{A}$	0.6	-	1.3	V
$I_{GSS}$	Gate Leakage Current	$V_{GS}=\pm 12\text{V}, V_{DS}=0\text{V}$	-	-	$\pm 100$	nA
$R_{DS(ON)}$	Drain-Source On-state Resistance	$V_{GS}=4.5\text{V}, I_{DS}=2.1\text{A}$	-	90	160	$\text{m}\Omega$
		$V_{GS}=2.5\text{V}, I_{DS}=1.5\text{A}$	-	154	200	
$G_{fs}$	Forward Transconductance	$V_{DS}=5\text{V}, I_D=2.1\text{A}$	-	10	-	S
<b>Body Diode Characteristics</b>						
$V_{SD}$	Diode Forward Voltage	$I_{SD}=1\text{A}, V_{GS}=0\text{V}$	-	0.8	1.0	V
<b>Dynamic Characteristics</b>						
$C_{iss}$	Input Capacitance	$V_{GS}=0\text{V}, V_{DS}=25\text{V},$ Frequency=1.0MHz	-	295	-	$\text{pF}$
$C_{oss}$	Output Capacitance		-	40	-	
$C_{rss}$	Reverse transfer capacitance		-	15	-	
$t_{d(ON)}$	Turn-on delay Time	$V_{GS}=4.5\text{V}, V_{DS}=27\text{V}$ $R_G=6\Omega, R_L=10\Omega, I_D=1\text{A}$	-	3.6	-	$\text{nS}$
$t_r$	Turn-on rise Time		-	3.5	-	
$t_{d(OFF)}$	Turn-off delay Time		-	32	-	
$t_f$	Turn-off rise Time		-	3	-	
<b>Gate Charge Characteristics</b>						
$Q_g$	Total Gate Charge	$V_{DS}=27\text{V}, V_{GS}=4.5\text{V},$ $I_{DS}=2.1\text{A}$	-	2.1	3.9	$\text{nC}$
$Q_{gs}$	Gate-Source Charge		-	0.6	-	
$Q_{gd}$	Gate-Drain Charge		-	0.8	-	

**TYPICAL CHARACTERISTICS (25 °C Unless Note)**

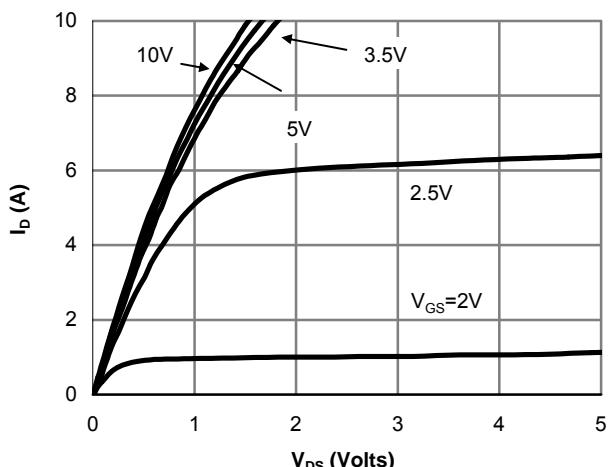


Fig 1: On-Region characteristics

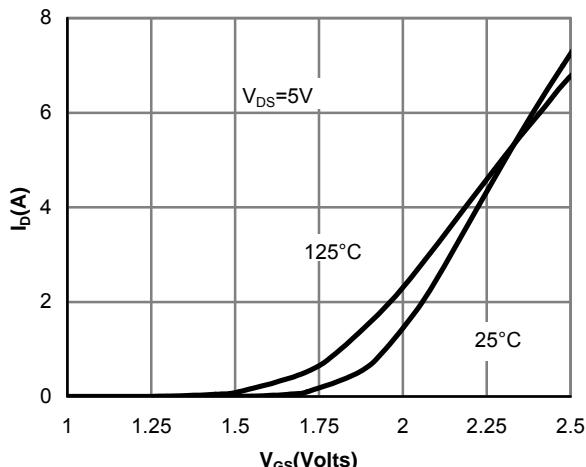


Figure 2: Transfer Characteristics

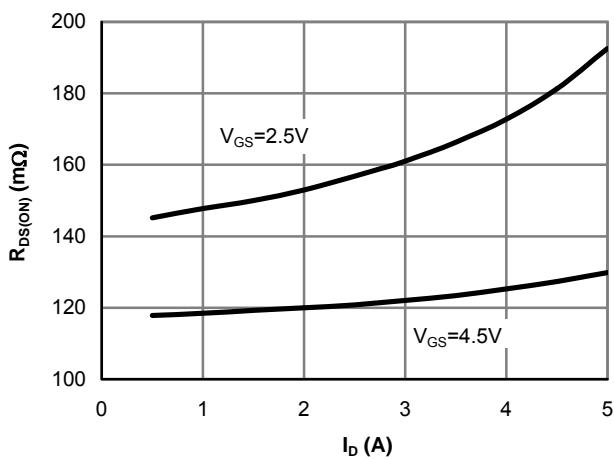


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

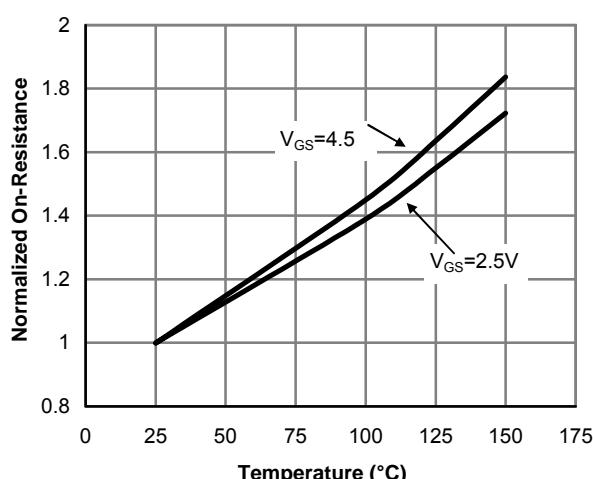


Figure 4: On-Resistance vs. Junction Temperature

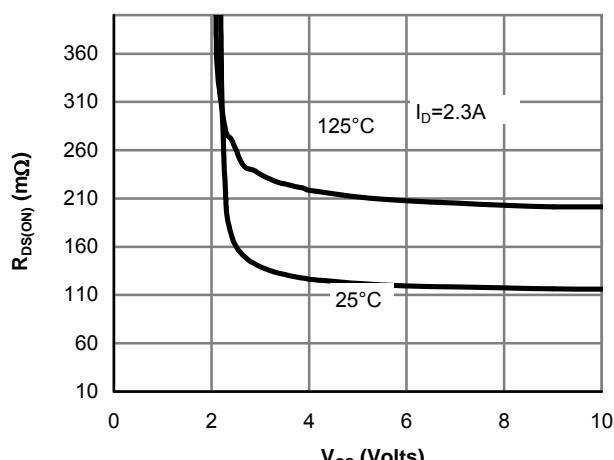


Figure 5: On-Resistance vs. Gate-Source Voltage

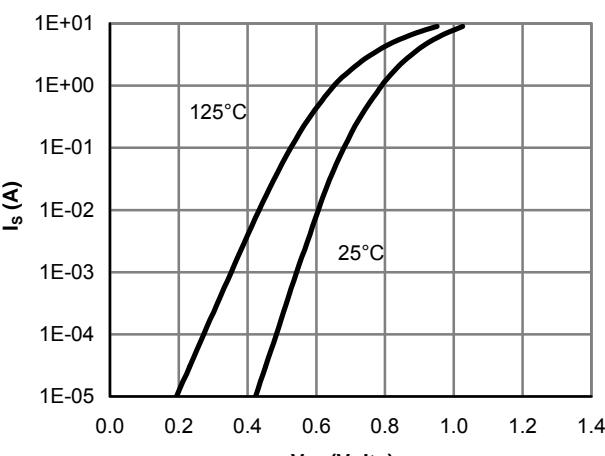


Figure 6: Body-Diode Characteristics

**TYPICAL CHARACTERISTICS (continuous)**

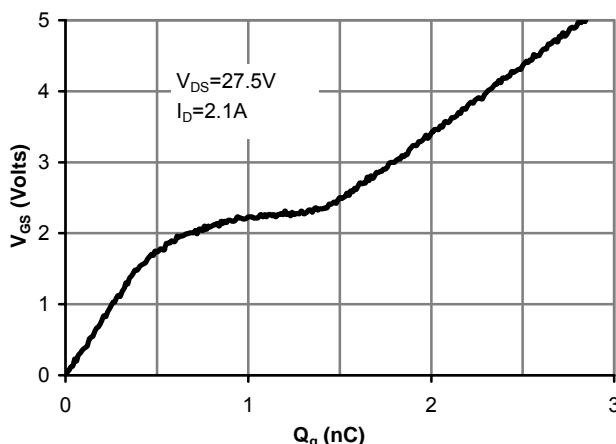


Figure 7: Gate-Charge Characteristics

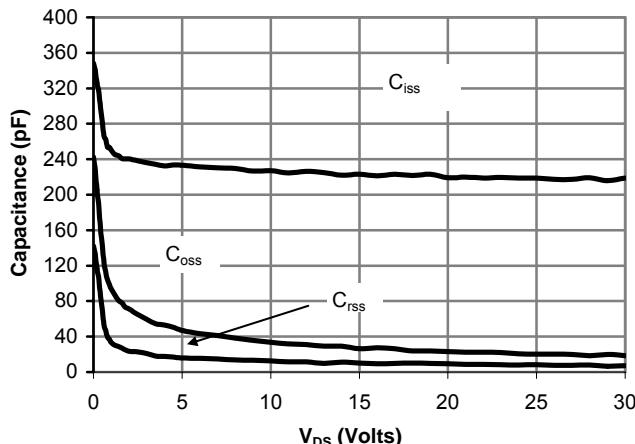


Figure 8: Capacitance Characteristics

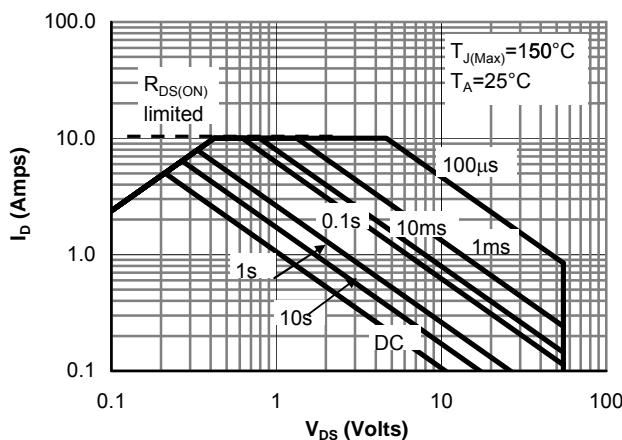


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

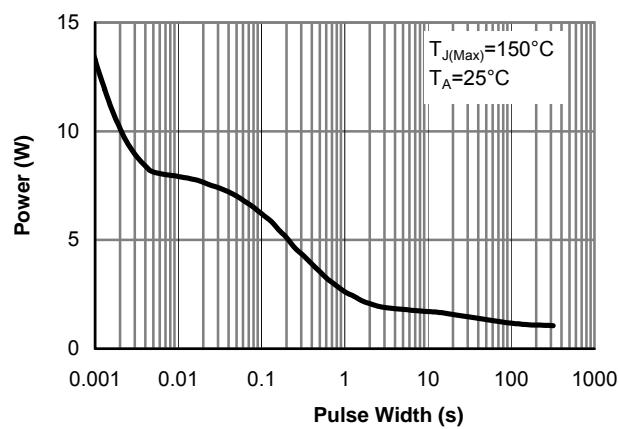


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

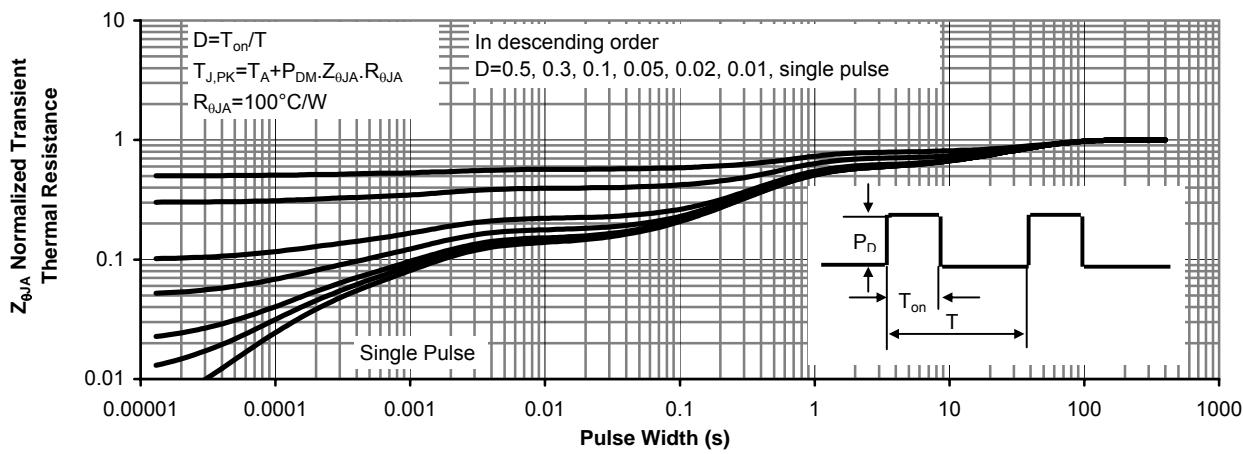
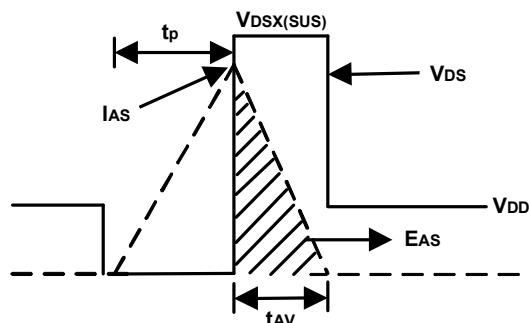
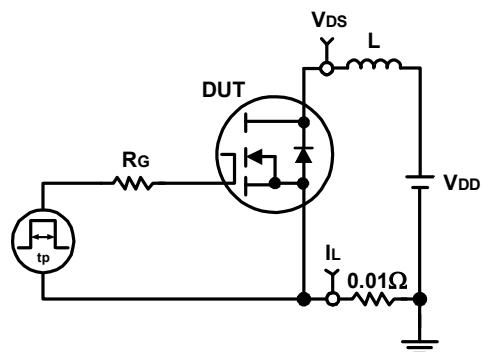
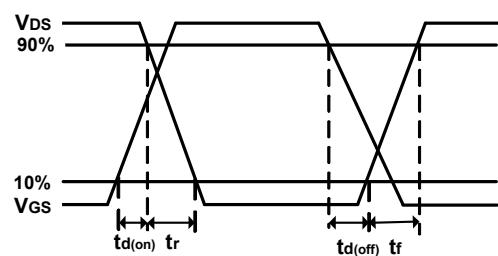
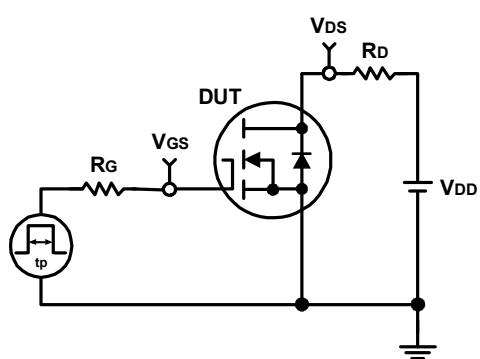


Figure 11: Normalized Maximum Transient Thermal Impedance

## Avalanche Test Circuit and Waveforms

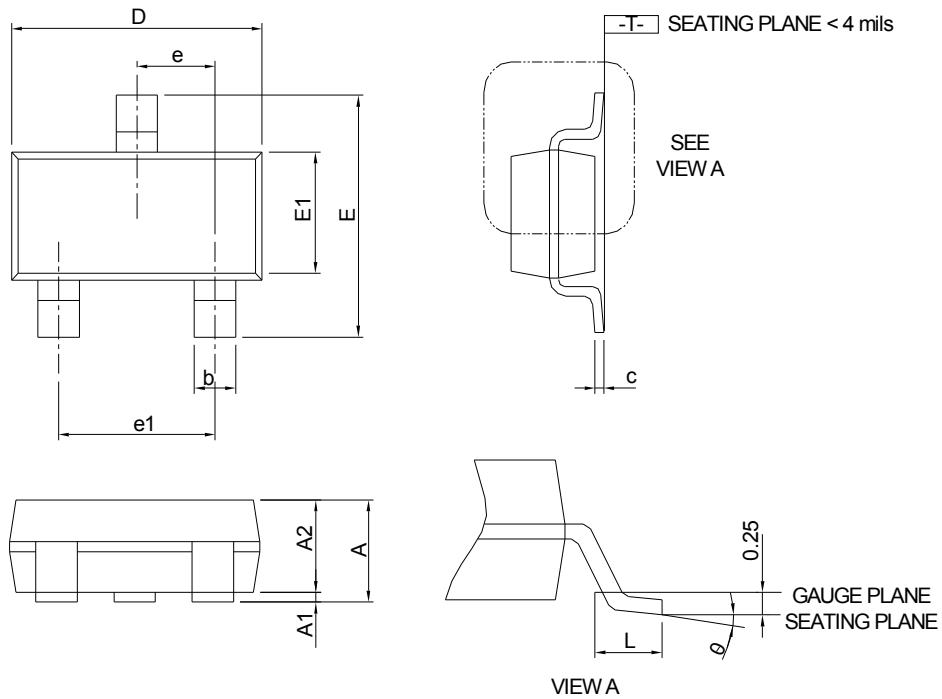


## Switching Time Test Circuit and Waveforms



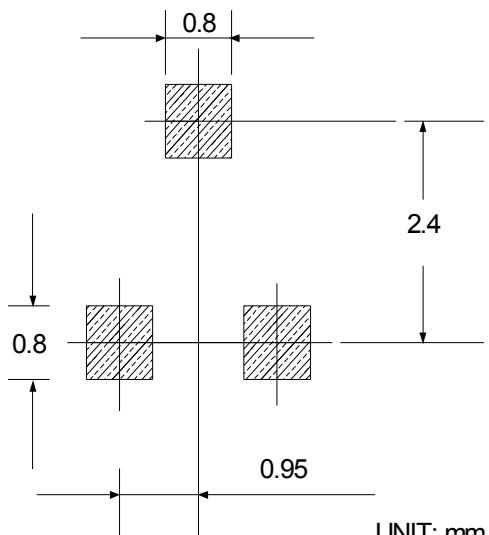
## Package Information

SOT23-3L



SYMBOL	SOT 23-3L			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.20		0.047
A1	0.00	0.08	0.000	0.003
A2	0.90	1.12	0.035	0.044
b	0.30	0.50	0.012	0.020
c	0.08	0.22	0.003	0.009
D	2.70	3.10	0.106	0.122
E	2.60	3.00	0.102	0.118
E1	1.40	1.80	0.055	0.071
e	0.95 BSC		0.037 BSC	
e1	1.90 BSC		0.075 BSC	
L	0.30	0.60	0.012	0.024
$\theta$	0°	8°	0°	8°

### RECOMMENDED LAND PATTERN



Note : Dimension D and E1 do not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 10 mil per side.

## Attention

- Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress rating only and functional device operation is not implied. YiDeng Wei Semiconductor assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all YiDeng Wei Semiconductor products described or contained herein.
- Any and all YiDeng Wei Semiconductor products described or contained herein do not have specifications that can handle applications that require extremely high levels of reliability, such as life-support systems, aircraft's control systems, or other applications whose failure can be reasonably expected to result in serious physical and/or material damage. Consult with your representative nearest you before using our products described or contained herein in such applications.
- YiDeng Wei Semiconductor strives to supply high-quality high-reliability products. However, any and all semiconductor products fail with some probability. It is possible that these probabilistic failures could give rise to accidents or events that could endanger human lives, that could give rise to smoke or fire, or that could cause damage to other property. When designing equipment, adopt safety measures so that these kinds of accidents or events cannot occur. Such measures include but are not limited to protective circuits and error prevention circuits for safe design, redundant design, and structural design.
- YiDeng Wei Semiconductor reserves the right to make modifications, enhancements, improvements, corrections or other changes without further notice to any product herein. YiDeng Wei Semiconductor does not assume any liability arising out of the application or use of any product described herein.